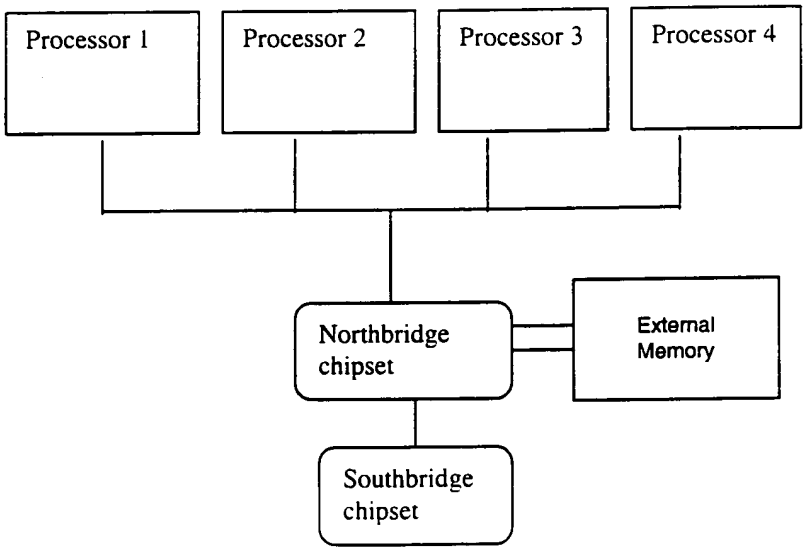

Processor 1
Processor 2
Processor 3
Processor 4
Northbridge chipset
External Memory
Southbridge chipset

Figure 1

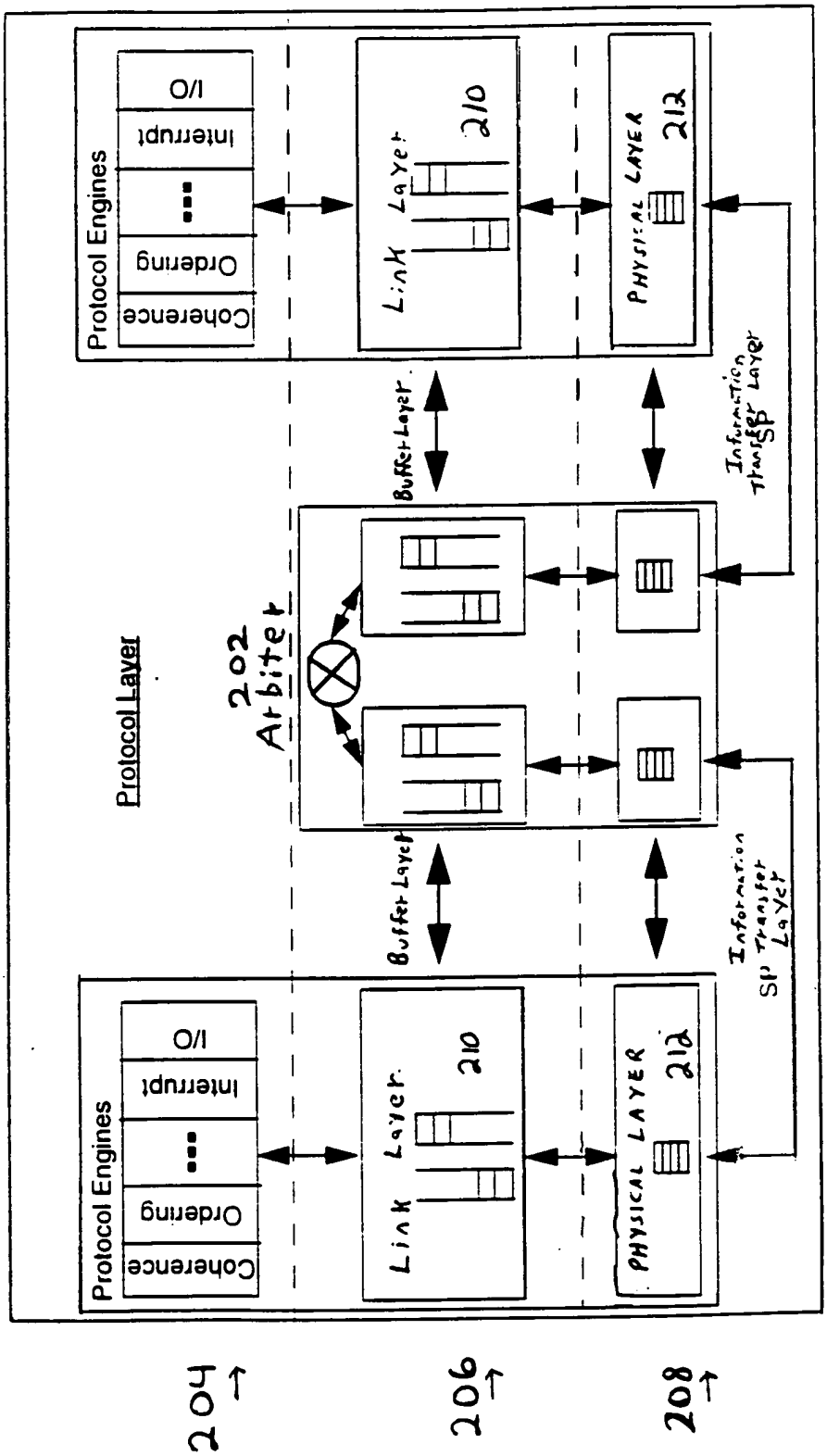

200
Protocol Layer
202
Arbiter
Protocol Engines
Coherence
Ordering
...
Interrupt
I/O
Link Layer
210
Physical Layer
212
Buffer Layer
Information SU Transfer Layer
204
206
208

Figure 2

Tosaeo Shezed

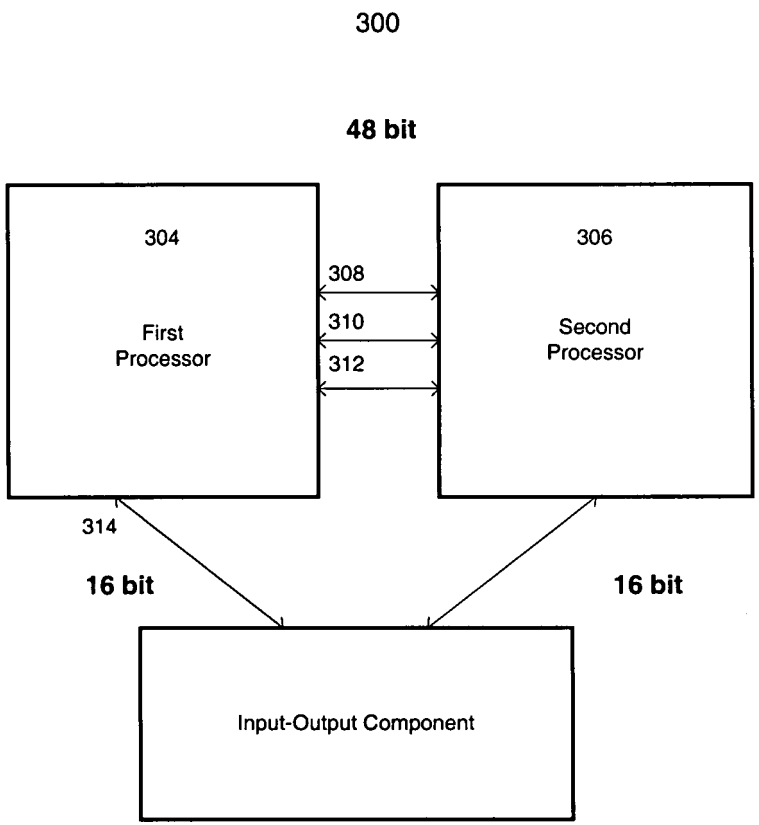


Figure 3

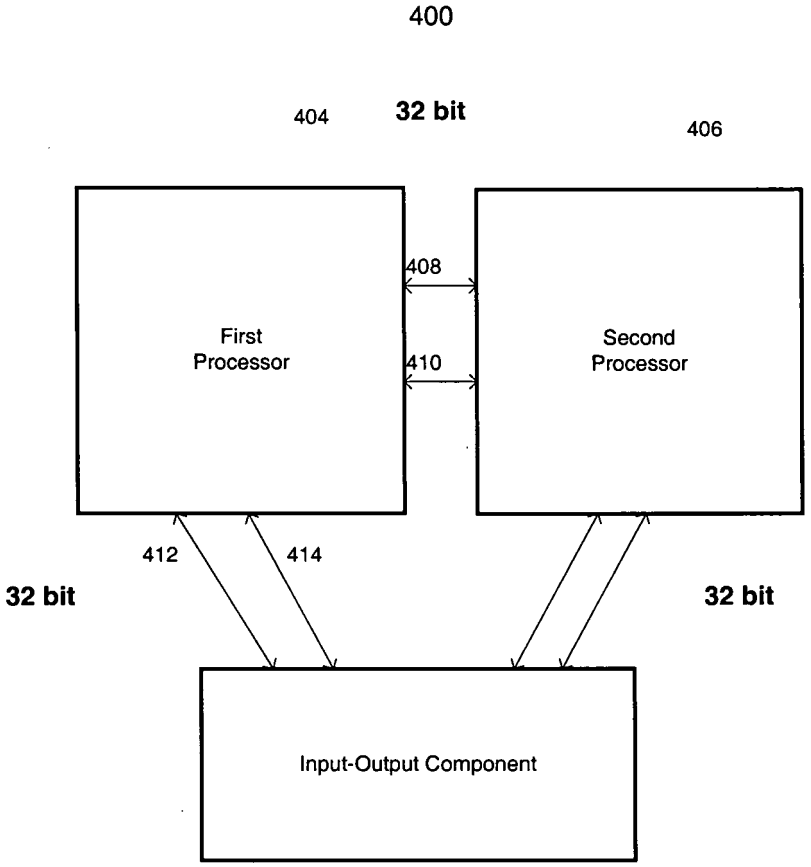


Figure 4

500

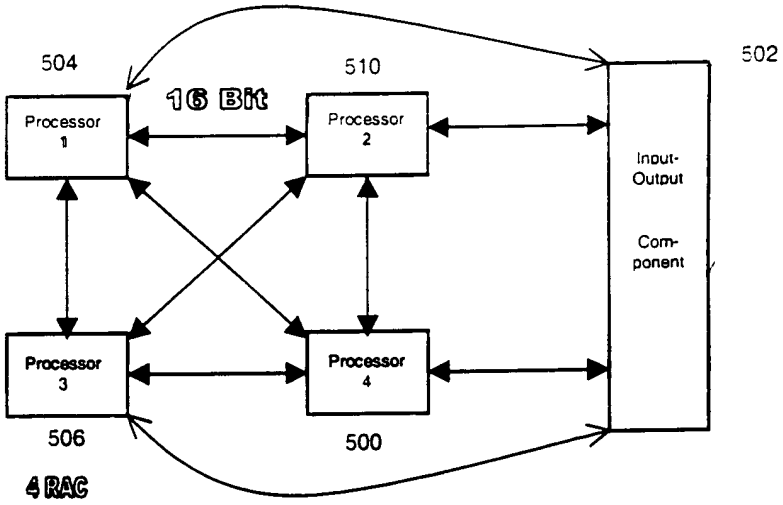
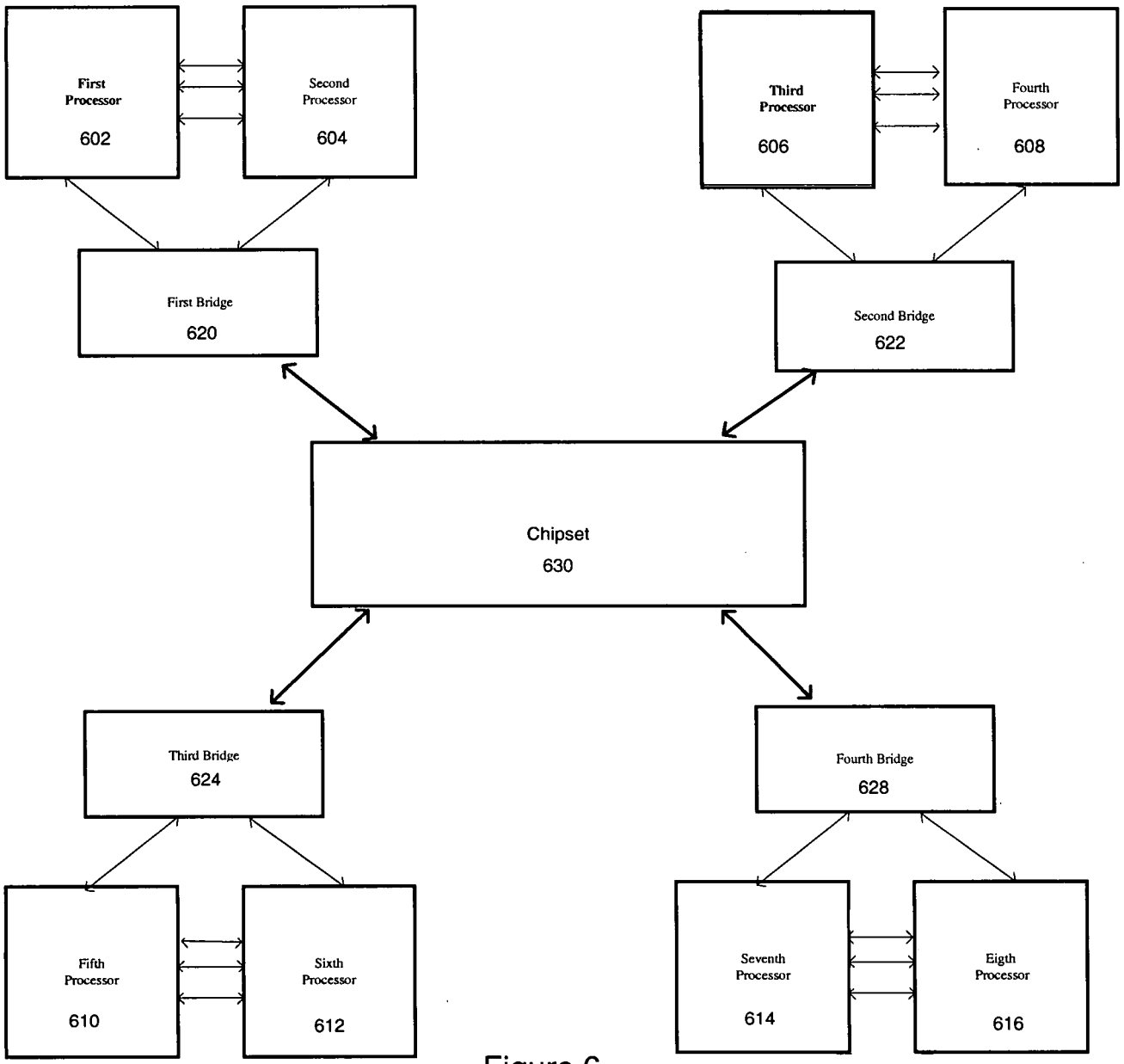

504
510
502
16 Bit
Processor 1
Processor 2
Input-Output
Com-ponent
Processor 3
Processor 4
506
500
4 RAC

Figure 5


First Processor 602
Second Processor 604
Third Processor 606
Fourth Processor 608
First Bridge 620
Second Bridge 622
Chipset 630
Third Bridge 624
Fourth Bridge 628
Fifth Processor 610
Sixth Processor 612
Seventh Processor 614
Eigth Processor 616

600

Figure 6

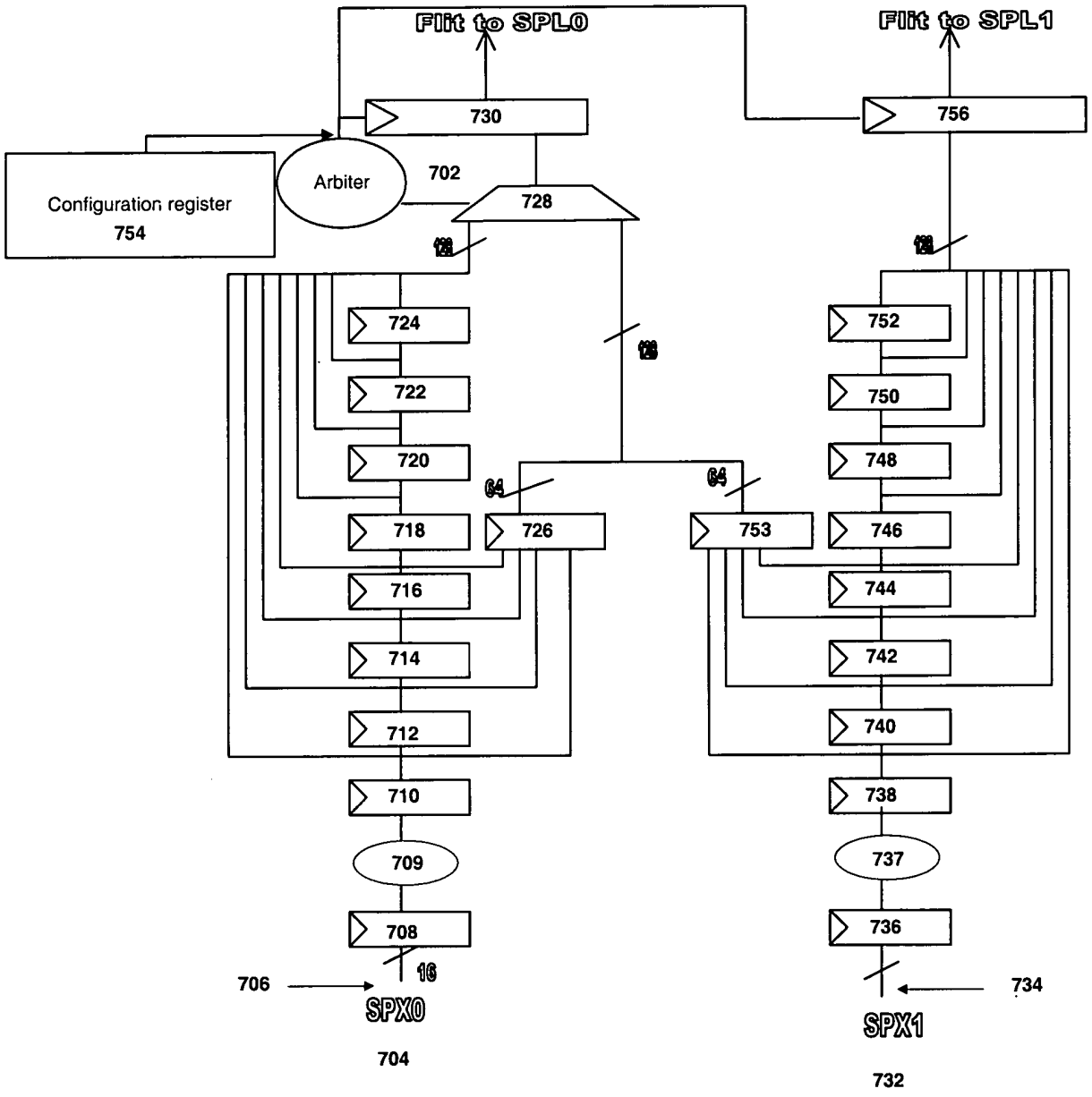
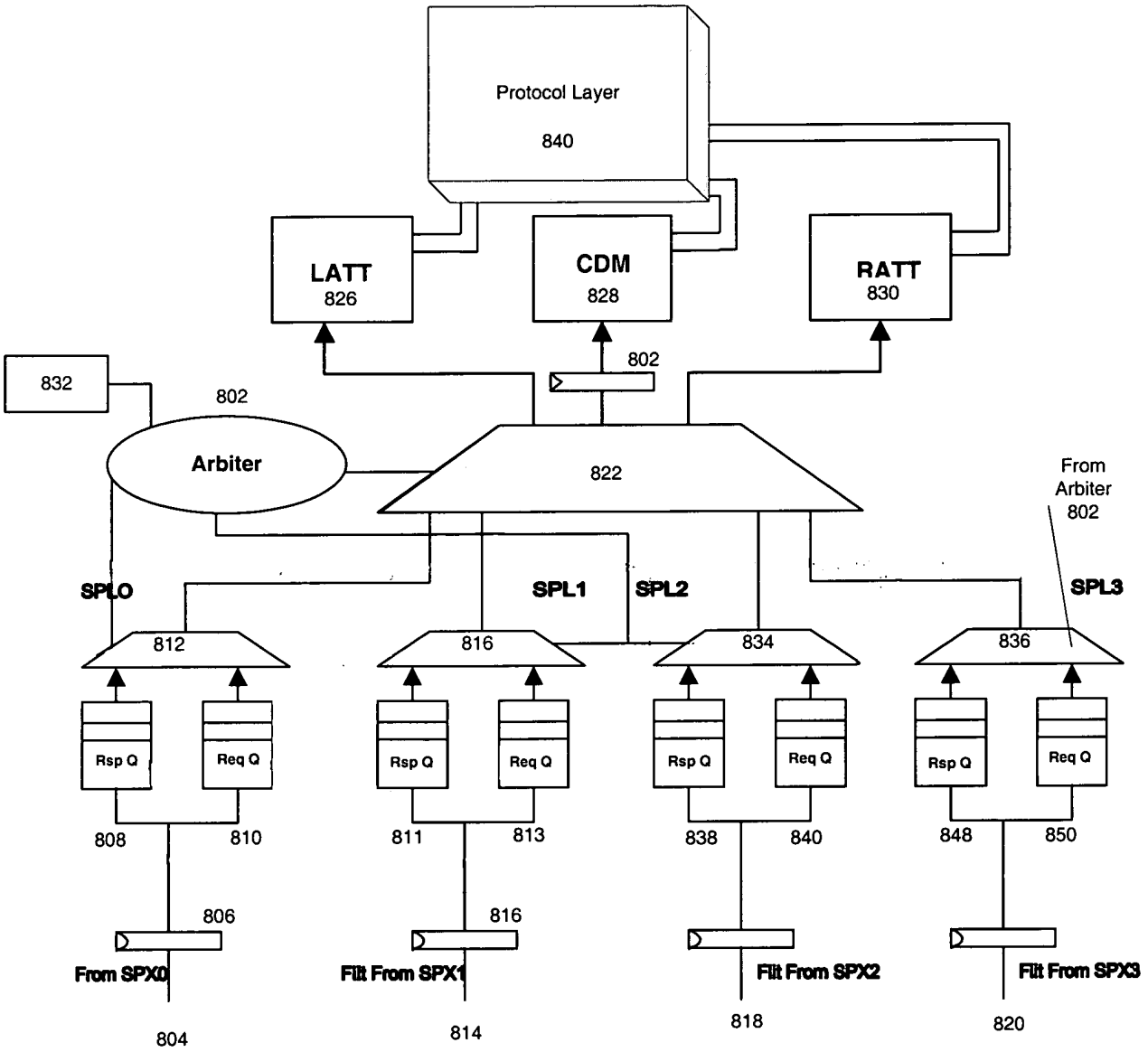

700
Flit to SPL0
Flit to SPL1
730
756
Arbiter
702
Configuration register
754
728
128
128
724
722
720
718
716
714
712
710
709
708
752
750
748
746
744
742
740
738
737
736
64
64
726
753
706
734
16
SPX0
SPX1
704
732

Figure 7


Protocol Layer
840
LATT
826
CDM
828
RATT
830
802
832
802
Arbiter
822
From
Arbiter
802
SPL0
SPL1
SPL2
SPL3
812
816
834
836
Rsp Q
Req Q
Rsp Q
Req Q
Rsp Q
Req Q
Rsp Q
Req Q
808
810
811
813
838
840
848
850
806
816
From SPX0
Flit From SPX1
Flit From SPX2
Flit From SPX3
804
814
818
820

800

Figure 8

TOSHIBA 0182269

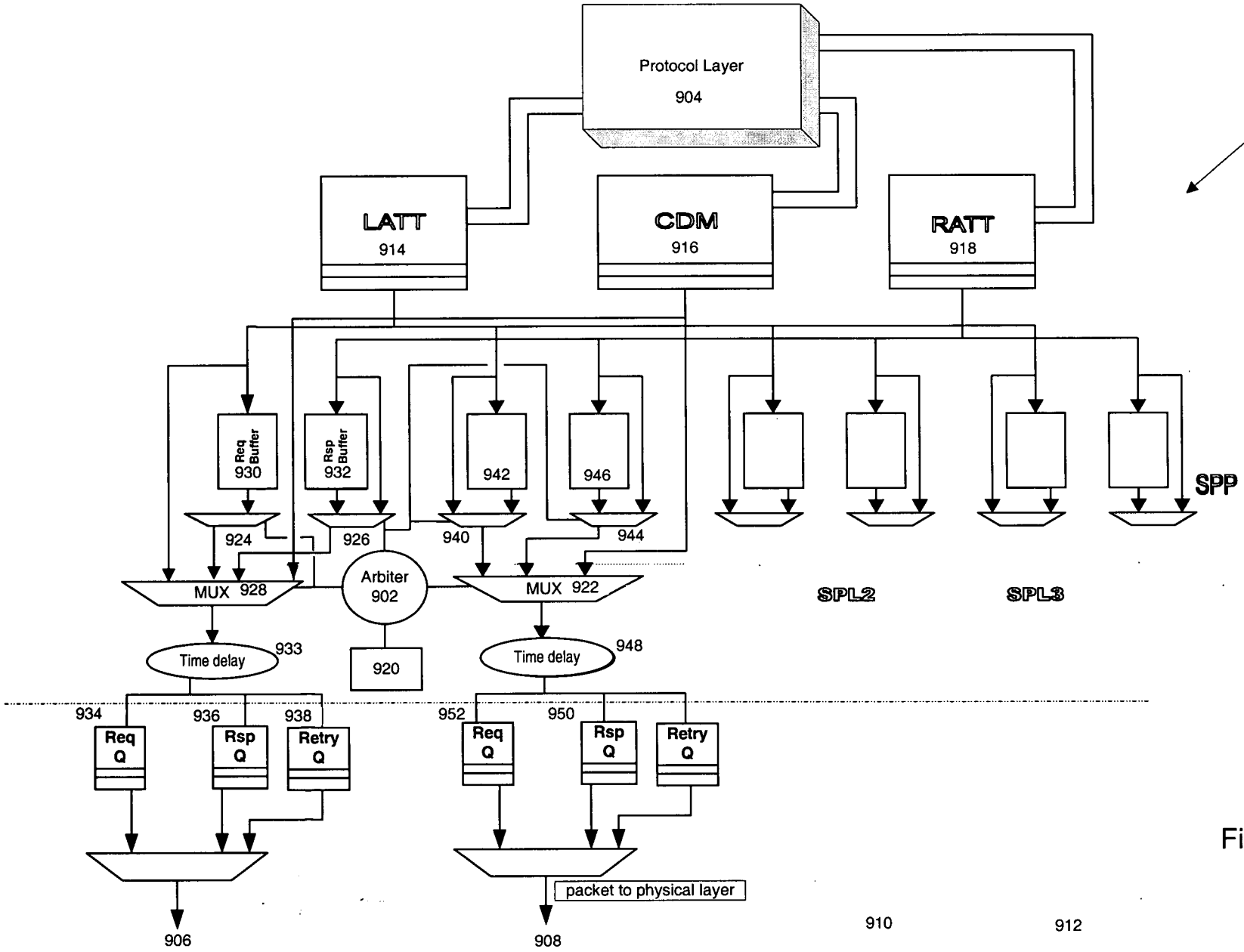


Figure 9

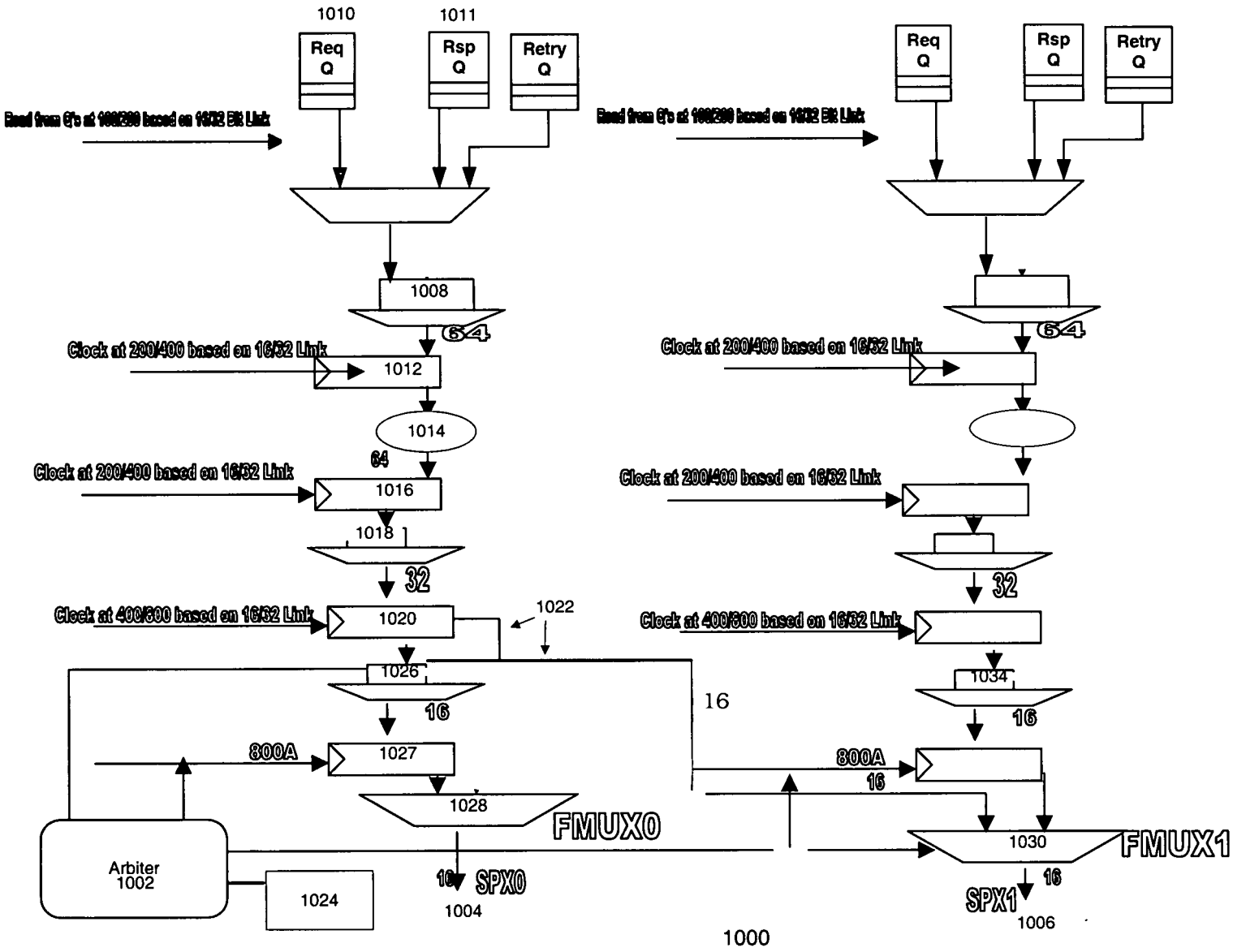

1010
1011
Req Q
Rsp Q
Retry Q
Req Q
Rsp Q
Retry Q
1008
64
64
Clock at 200/400 based on 16/32 Link
1012
Clock at 200/400 based on 16/32 Link
1014
64
Clock at 200/400 based on 16/32 Link
1016
Clock at 200/400 based on 16/32 Link
1018
32
32
Clock at 400/800 based on 16/32 Link
1020
1022
Clock at 400/800 based on 16/32 Link
1026
16
1034
16
16
800A
1027
800A
16
1028
FMUX0
1030
FMUX1
Arbiter 1002
1024
16
SPX0
1004
SPX1
16
1006
1000
1031
1032

Figure 10